Department of Materials

Nanotechnology Centre

HIGH FREQUENCY CHARACTERISATION OF MN DOPED SOL GEL $Pb_xSr_{1-x}TiO_3$ METAL-INSULATOR-METAL CAPACITORS FOR FREQUENCY AGILE APPLICATIONS

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Introduction

•Frequency agile materials offer large variation in dielectric constant with applied electric field, which makes them ideal candidates for passive components with potentially high tunability and low loss

•Increasing interest in $Pb_xSr_{1-x}TiO_3$ (PST). Investigation of doping of PST with Mn, using the sol-gel technique, and its potential use for the realization of microwave components.

▪Sol-gel deposition method

▪Deposition over large area - Ease of doping - Low cost - Relatively low annealing temperature

•Good quality, uniform films at relatively low temperatures depending on the composition

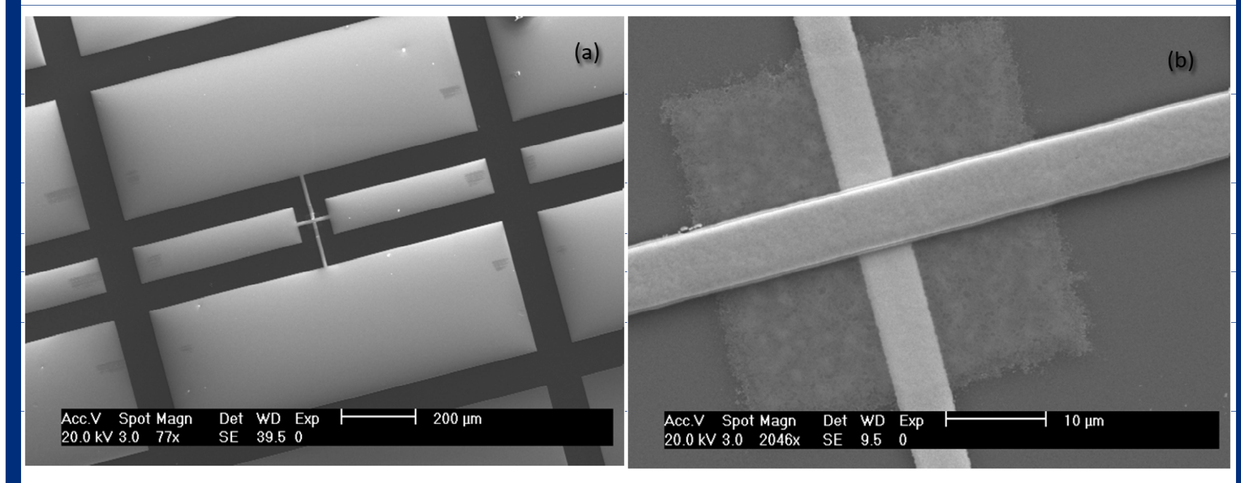

Figure 1. (a) Overview and (b) Close-up *optical micrographs of a fabricated 5 um X 5 um CPW MIM shunt capacitor*

Experiments

Fabrication process.

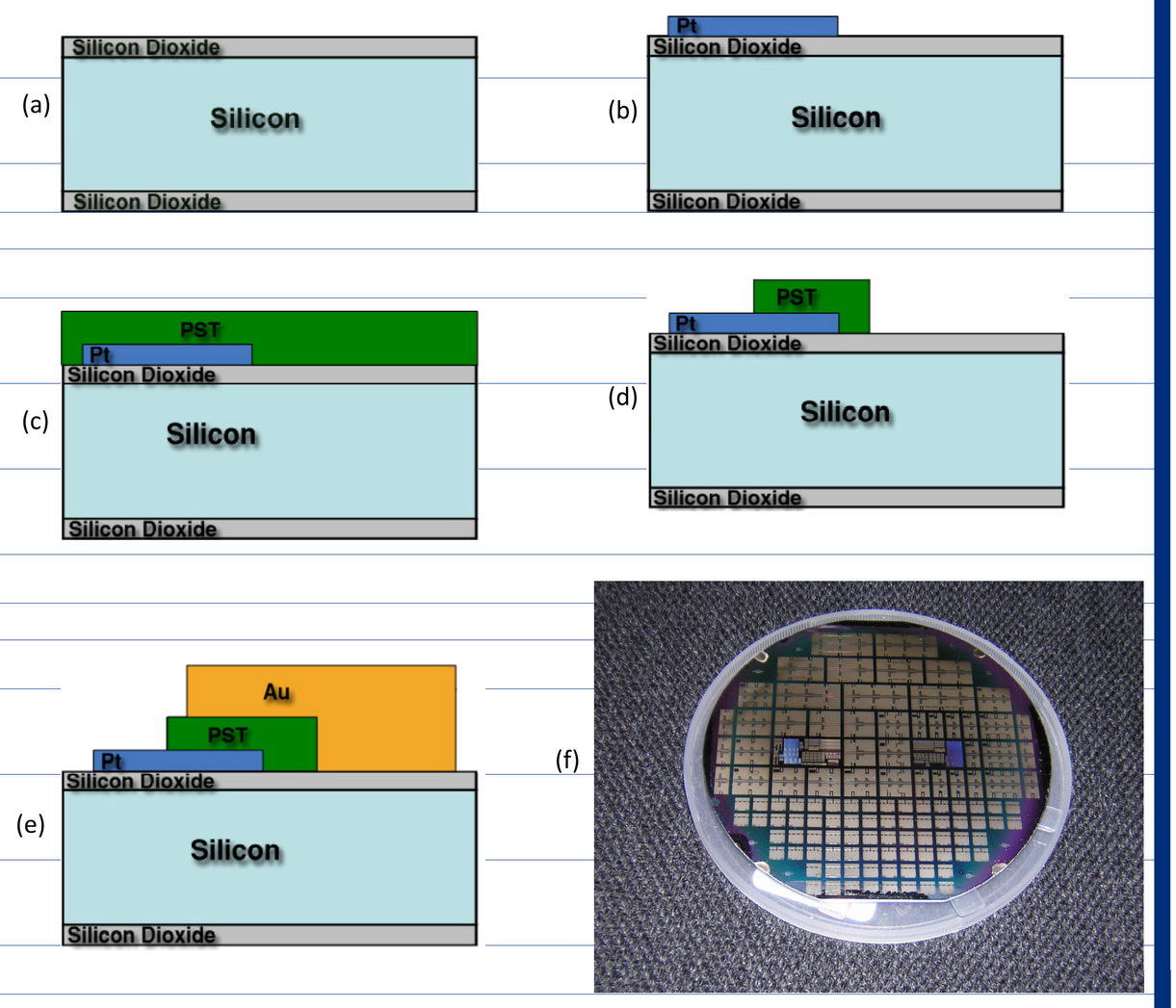

Figure 2. Fabrication process. (a) SiO_2 substrate, (b) Platinum deposition and patterning via lift-off, (c) sol-gel deposition of PST, (d) patterning of PST using wet-etching, (e) deposition of top electrode using electroplating, (f) digital picture of a 4-inch fabricated Silicon wafer containing PST MIM capacitors

High frequency characterisation

S-parameter measurements

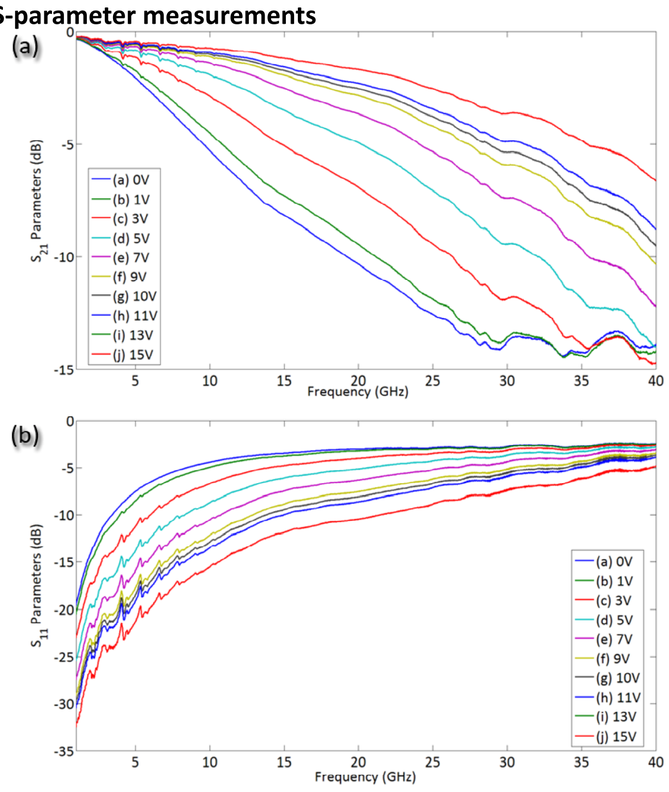

Figure 3. Measured (a) insertion and (b) return loss of *a fabricated 5 um X 5 um CPW Si MIM shunt capacitor with 300 nm of PST, applying 0 – 15 Volts*

Extracted parameters – MIM capacitor on sapphire substrate

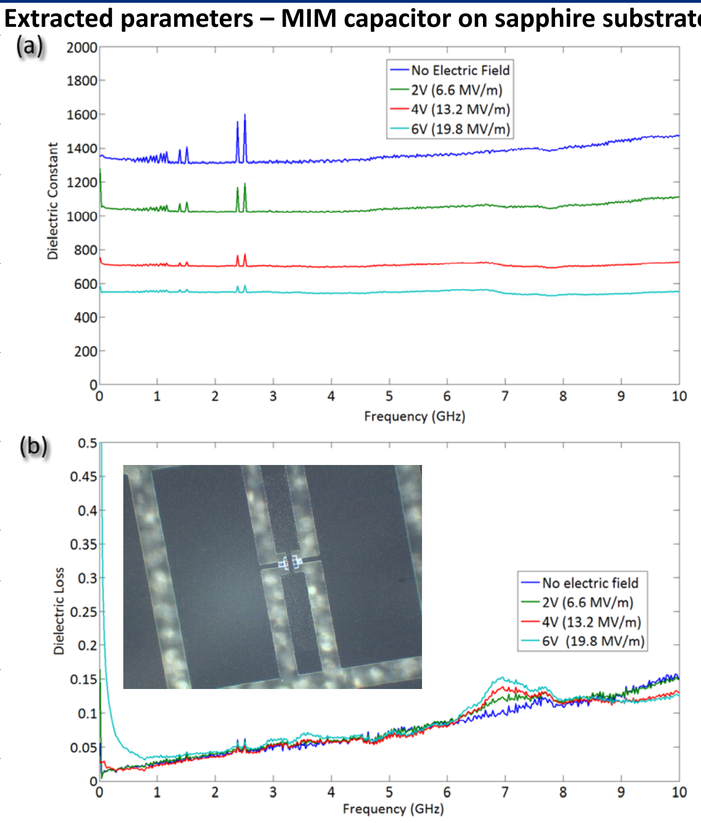

Figure 5. Extracted (a) dielectric constant and (b) loss of *a fabricated 5 um X 5 um CPW MIM series capacitor with 300 nm of PST on sapphire, applying 0 – 6 Volts*

Extracted parameters – MIM capacitor on silicon substrate

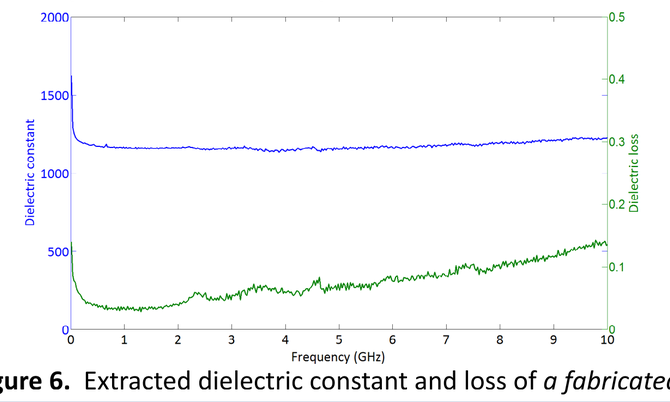

Figure 6. Extracted dielectric constant and loss of *a fabricated 5 um X 5 um CPW Si MIM capacitor with 300 nm of PST on silicon – no electric field applied*

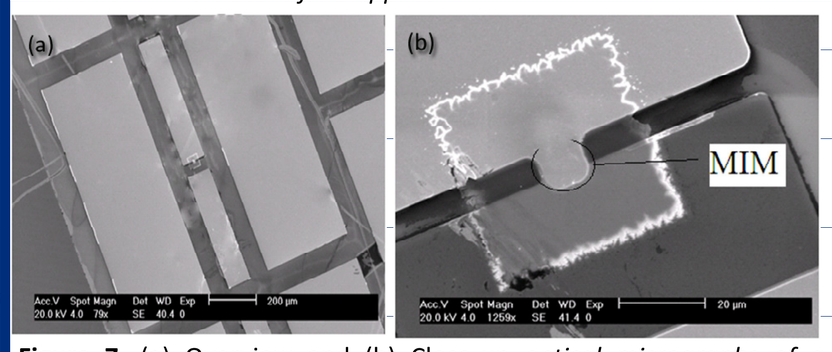

Figure 7. (a) Overview and (b) Close-up *optical micrographs of a fabricated 5 um X 5 um CPW MIM series capacitor on silicon*

Extraction technique

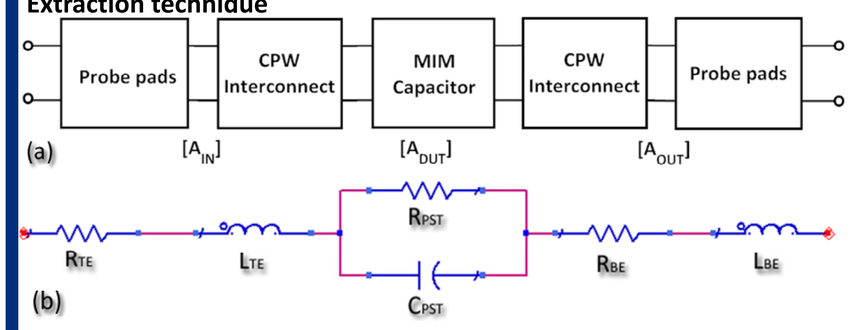

Figure 4. (a) De-embedding of interconnects and probe pads capacitance to extract the "pure" performance of the PST MIM capacitor, (b) lumped element equivalent of MIM capacitor is fitted to S/Y-parameter measurements

Conclusions

•Crack free PST films with good surface morphology were achieved, enabling the fabrication of structures with smooth features and high definition.

•Fabrication process of CPW MIM capacitors with PST was established on silicon and sapphire substrates.

•De-embedding and lumped element fitting algorithm of measured S-parameters realized using MATLAB.

•Ongoing work involves further investigation on PST compositions.

Acknowledgements

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Selected References

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